AMENDMENTS TO THE CLAIMS:

Please amend claims 1, 4, 8, 23 and 30 as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) Apparatus for processing data, said apparatus comprising:

a processing circuit having a power supply configuration and driven by a clock signal, said processing circuit ~~being operable~~including:

(i) ~~in~~ a processing mode ~~to perform~~for performing data processing operations when said power supply configuration has a processing configuration and said clock signal is clocked; and

(ii) ~~in~~ a holding mode ~~to hold~~for holding state without performing data processing operations when said power supply has a holding configuration and said clock signal is stopped; and

a power supply and clock signal control circuit, responsive to a target rate signal indicative of a target rate of data processing operations to be performed by said processing circuit, to modulate a target rate mode control signal to switch said processing circuit between said processing mode and said holding mode so as to achieve said target rate.

2. (original) Apparatus as claimed in claim 1, comprising one or more further circuits coupled to said processing circuit.

3. (original) Apparatus as claimed in claim 1, wherein said processing circuit is operable to generate a busy signal indicative of whether said processing circuit can be switched from said

processing mode to said holding mode, said power supply and clock signal control circuit being responsive to said busy signal to override said target rate mode control signal to prevent a switch of said processing circuit from said processing mode to said holding mode independent of said target rate.

4. (currently amended) Apparatus as claimed in claim ~~2~~3, wherein said processing circuit is operable to assert said busy signal when a signal transfer is pending between said processing circuit and at least one of said one or more further circuits.

5. (original) Apparatus as claimed in claim 1, wherein said power supply and clock signal control circuit is responsive to a priority signal to override said target rate mode control signal to:

(i) switch said processing circuit from said holding mode to said processing mode independent of said target rate; and

(ii) to prevent a switch of said processing circuit from said processing mode to said holding mode independent of said target rate.

6. (original) Apparatus as claimed in claim 5, wherein said priority signal is one of:

(i) an interrupt signal; and

(ii) a hardware real-time timer signal.

7. (original) Apparatus as claimed in claim 1, wherein said target rate mode control signal, said busy signal and said priority signal are logically combined to generate a signal operable to switch said processing circuit between said processing mode and said holding mode.

8. (currently amended) Apparatus as claimed in claim 1, wherein said holding configuration corresponds to a power supply to said processing circuit having a potential difference lower than said potential difference corresponding to said processing configuration.

9. (original) Apparatus as claimed in claim 8, wherein said processing circuit has a lower power consumption configuration when in said holding mode than when in said processing mode.

10. (original) Apparatus as claimed in claim 8, wherein in said holding mode said potential difference of said power supply to said processing circuit is insufficient to allow said processing circuit to be clocked.

11. (original) Apparatus as claimed in claim 2, wherein one or more signal clamping circuits are provided between said processing circuit and said one or more further circuits.

12. (original) Apparatus as claimed in claim 1, wherein said processing circuit is a processor core.

13. (original) Apparatus as claimed in claim 2, wherein active high signalling is used from said processing circuit and said one or more further circuits.

14. (original) Apparatus as claimed in claim 1, comprising a clock generator operable to generate a clock source signal having a fixed frequency which is selectively supplied to said processing circuit in dependence upon whether said processing circuit is in said processing mode or said holding mode.

15. (original) Apparatus as claimed in claim 14, comprising a power supply generator, wherein when switching from said holding mode to said processing mode, said power supply generator sends a ready signal to said clock generator to indicate that said power supply configuration has reached said processing configuration such that said clock signal may be started.

16. (original) A method of processing data, said method comprising the steps of:

operating a processing circuit powered by a power supply signal and driven by a clock signal such that:

(i) in a processing mode said processing circuit performs data processing operations when said power supply signal has a processing configuration and said clock signal is clocked; and

(ii) in a holding mode said processing circuit holds state without performing data processing operations when said power supply has a holding configuration and said clock signal is stopped; and

in response to a target rate signal indicative of a target rate of data processing operations to be performed by said processing circuit using a power supply and clock signal control circuit to modulate a target rate mode control signal to switch said processing circuit between said processing mode and said holding mode so as to achieve said target rate.

17. (original) A method as claimed in claim 16, wherein one or more further circuits are coupled to said processing circuit.

18. (original) A method as claimed in claim 16, wherein said processing circuit is operable to generate a busy signal indicative of whether said processing circuit can be switched from said processing mode to said holding mode, said power supply and clock signal control circuit being responsive to said busy signal to override said target rate mode control signal to prevent a switch of said processing circuit from said processing mode to said holding mode independent of said target rate.

19. (original) A method as claimed in claim 17, wherein said processing circuit is operable to assert said busy signal when a signal transfer is pending between said processing circuit and at least one of said one or more further circuits.

20. (original) A method as claimed in claim 16, wherein said power supply and clock signal control circuit is responsive to a priority signal to override said target rate mode control signal to:

(i) switch said processing circuit from said holding mode to said processing mode independent of said target rate; and

(ii) to prevent a switch of said processing circuit from said processing mode to said holding mode independent of said target rate.

21. (original) A method as claimed in claim 20, wherein said priority signal is one of:

(i) an interrupt signal; and

(ii) a hardware real-time timer signal.

22. (original) A method as claimed in claim 16, wherein said target rate mode control signal, said busy signal and said priority signal are logically combined to generate a signal operable to switch said processing circuit between said processing mode and said holding mode.

23. (currently amended) A method as claimed in claim 16, wherein said holding configuration corresponds to a power supply to said processing circuit having a potential difference lower than said potential difference corresponding to said processing configuration.

24. (original) A method as claimed in claim 23, wherein said processing circuit has a lower power consumption when in said holding mode than when in said processing mode.

25. (original) A method as claimed in claim 23, wherein in said holding mode said potential difference of said power supply to said processing circuit is insufficient to allow said processing circuit to be clocked.

26. (original) A method as claimed in claim 17, wherein one or more signal clamping circuits are provided between said processing circuit and said one or more further circuits.

27. (original) A method as claimed in claim 16, wherein said processing circuit is a processor core.

28. (original) A method as claimed in claim 17, wherein active high signalling is used from said processing circuit and said one or more further circuits.

29. (original) A method as claimed in claim 16, wherein a clock generator is operable to generate a clock source signal having a fixed frequency which is selectively supplied to said processing circuit in dependence upon whether said processing circuit is in said processing mode or said holding mode.

30. (currently amended) ~~Apparatus~~Method as claimed in claim 29, wherein when switching from said holding mode to said processing mode, a power supply generator sends a ready signal to said clock generator to indicate that said power supply configuration has reached said processing configuration such that said clock signal may be started.